

## CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

5           1.     A semiconductor device, comprising:

          a P-type semiconductor substrate;

          a P-channel DMOS transistor disposed on the P-type semiconductor substrate and including a drain formed of the P-type semiconductor substrate and a source formed in the P-type semiconductor substrate on a main surface of the P-type semiconductor substrate; and

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          a CMOS transistor disposed on the P-type semiconductor substrate and including a P-channel MOS transistor formed in an N-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate and an N-channel MOS transistor formed in a P-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from the P-type semiconductor substrate by the N-type region.

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          2.     The semiconductor device as defined in Claim 1, wherein the P-type semiconductor substrate comprises a P-type high concentration semiconductor substrate and a first P-type low concentration epitaxial layer, the P-type high concentration semiconductor substrate being disposed opposite

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to the main surface of the P-type semiconductor substrate,  
and the first P-type low concentration epitaxial layer being  
disposed over the P-type high concentration semiconductor  
substrate.

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3. The semiconductor device as defined in Claim 2,  
wherein the N-type region comprises a bottom portion  
including an N-type buried layer which is disposed at an  
interface of the P-type high concentration semiconductor  
10 substrate and the first P-type low concentration epitaxial  
layer.

4. The semiconductor device as defined in Claim 3,  
wherein the N-type region further comprises at least two side  
15 portions, each including an Nwell region, to form a structure  
such that the P-type region is surrounded by the Nwell  
regions and the N-type buried layer.

5. The semiconductor device as defined in Claim 2,  
20 wherein the first P-type low concentration epitaxial layer  
includes a P-type buried layer disposed under a region where  
the source of the P-channel DMOS transistor is formed.

6. A semiconductor device, comprising:  
25 a P-type semiconductor substrate including a P-type  
high concentration semiconductor substrate, a first P-type

low concentration epitaxial layer, and a second P-type low concentration epitaxial layer, the P-type high concentration semiconductor substrate being disposed opposite to the main surface of the P-type semiconductor substrate, the second P-type low concentration epitaxial layer being disposed over the P-type high concentration semiconductor substrate, and the first P-type low concentration epitaxial layer being disposed over the second P-type low concentration epitaxial layer;

10           a P-channel DMOS transistor disposed on the P-type semiconductor substrate and including a drain formed of the P-type semiconductor substrate and a source formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate; and

15           a CMOS transistor disposed on the P-type semiconductor substrate and including a P-channel MOS transistor formed in an N-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate and an N-channel MOS transistor formed in a P-type region formed  
20 in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from the P-type semiconductor substrate by the N-type region,

          wherein the N-type region comprises a bottom portion  
25 including an N-type buried layer which is disposed at an interface of the first P-type low concentration epitaxial

layer and the second P-type low concentration epitaxial layer.

7. A semiconductor device, comprising:

a P-type semiconductor substrate including a P-type  
5 high concentration semiconductor substrate, a first P-type  
low concentration epitaxial layer, a second P-type low  
concentration epitaxial layer, and a third P-type low  
concentration epitaxial layer, the P-type high concentration  
semiconductor substrate being disposed opposite to the main  
10 surface of the P-type semiconductor substrate, the second P-  
type low concentration epitaxial layer being disposed over  
the P-type high concentration semiconductor substrate, the  
third P-type low concentration epitaxial layer being disposed  
over the second P-type low concentration epitaxial layer, and  
15 the first P-type low concentration epitaxial layer being  
disposed over the third P-type low concentration epitaxial  
layer;

a P-channel DMOS transistor disposed on the P-type  
semiconductor substrate and including a drain formed of the  
20 P-type semiconductor substrate and a source formed in the P-  
type semiconductor substrate on the main surface of the P-  
type semiconductor substrate; and

a CMOS transistor disposed on the P-type semiconductor  
substrate and including a P-channel MOS transistor formed in  
25 an N-type region formed in the P-type semiconductor substrate  
on a main surface of the P-type semiconductor substrate and

an N-channel MOS transistor formed in a P-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from the P-type semiconductor substrate  
5 by the N-type region,

wherein the N-type region comprises a bottom portion including an N-type buried layer which is disposed at an interface of the second P-type low concentration epitaxial layer and the third P-type low concentration epitaxial layer,  
10 and the P-type region comprises a bottom portion including a P-type buried layer which is disposed at an interface of the first P-type low concentration epitaxial layer and the third P-type low concentration epitaxial layer.

15 8. A semiconductor device, comprising:

an N-type semiconductor substrate;

an N-channel DMOS transistor disposed on the N-type semiconductor substrate and including a drain formed of the N-type semiconductor substrate and a source formed in the N-type semiconductor substrate on a main surface of the N-type semiconductor substrate; and  
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a CMOS transistor disposed on the N-type semiconductor substrate and including an N-channel MOS transistor formed in a P-type region formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate and  
25 a P-channel MOS transistor formed in an N-type region formed

in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate, the N-type region being electrically isolated from the N-type semiconductor substrate by the P-type region.

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9. The semiconductor device as defined in Claim 8, wherein the N-type semiconductor substrate comprises an N-type high concentration semiconductor substrate and a first N-type low concentration epitaxial layer, the N-type high concentration semiconductor substrate being disposed opposite to the main surface of the N-type semiconductor substrate, and the first N-type low concentration epitaxial layer being disposed over the N-type high concentration semiconductor substrate.

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10. The semiconductor device as defined in Claim 9, wherein the P-type region comprises a bottom portion including a P-type buried layer which is disposed at an interface of the N-type high concentration semiconductor substrate and the first N-type low concentration epitaxial layer.

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11. The semiconductor device as defined in Claim 10, wherein the P-type region further comprises at least two side portions, each including an Pwell region, to form a structure such that the N-type region is surrounded by the Pwell

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regions and the P-type buried layer.

12. The semiconductor device as defined in Claim 9,  
wherein the first N-type low concentration epitaxial layer  
5 includes an N-type buried layer disposed under a region where  
the source of the N-channel DMOS transistor is formed.

13. A semiconductor device, comprising:

an N-type semiconductor substrate including an N-type  
10 high concentration semiconductor substrate, a first N-type  
low concentration epitaxial layer, and a second N-type low  
concentration epitaxial layer, the N-type high concentration  
semiconductor substrate being disposed opposite to a main  
surface of the N-type semiconductor substrate, the second N-  
15 type low concentration epitaxial layer being disposed over  
the N-type high concentration semiconductor substrate, and  
the first N-type low concentration epitaxial layer being  
disposed over the second N-type low concentration epitaxial  
layer;

20 an N-channel DMOS transistor disposed on the N-type  
semiconductor substrate and including a drain formed of the  
N-type semiconductor substrate and a source formed in the N-  
type semiconductor substrate on the main surface of the N-  
type semiconductor substrate; and

25 a CMOS transistor disposed on the N-type semiconductor  
substrate and including an N-channel MOS transistor formed in

a P-type region formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate and a P-channel MOS transistor formed in an N-type region formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate, the N-type region being electrically isolated from the N type semiconductor substrate by the P-type region,

wherein the P-type region comprises a bottom portion including a P-type buried layer which is disposed at an interface of the first N-type low concentration epitaxial layer and the second N-type low concentration epitaxial layer.

14. A semiconductor device, comprising:

an N-type semiconductor substrate including an N-type high concentration semiconductor substrate, a first N-type low concentration epitaxial layer, a second N-type low concentration epitaxial layer, and a third N-type low concentration epitaxial layer, the N-type high concentration semiconductor substrate being disposed opposite to a main surface of the N-type semiconductor substrate, the second N-type low concentration epitaxial layer being disposed over the N-type high concentration semiconductor substrate, the third N-type low concentration epitaxial layer being disposed over the second N-type low concentration epitaxial layer, and the first N-type low concentration epitaxial layer being disposed over the third N-type low concentration epitaxial



layer;

an N-channel DMOS transistor disposed on the N-type semiconductor substrate and including a drain formed of the N-type semiconductor substrate and a source formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate; and

a CMOS transistor disposed on the N-type semiconductor substrate and including an N-channel MOS transistor formed in a P-type region formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate and a P-channel MOS transistor formed in an N-type region formed in the N-type semiconductor substrate on the main surface of the N-type semiconductor substrate, the N-type region being electrically isolated from the N-type semiconductor substrate by the P-type region,

wherein the P-type region comprises a bottom portion including a P-type buried layer which is disposed at an interface of the second N-type low concentration epitaxial layer and the third N-type low concentration epitaxial layer, and the N-type buried layer is disposed on a bottom of the N-type region disposed at an interface of the first N-type low concentration epitaxial layer and the third N-type low concentration epitaxial layer.

15. A semiconductor device comprising:  
a fixed voltage circuit comprising:

a P-type semiconductor substrate;

an output transistor including a P-channel DMOS transistor disposed on the P-type semiconductor substrate and including a drain formed of the P-type semiconductor substrate and a  
5 source formed in the P-type semiconductor substrate on a main surface of the P-type semiconductor substrate; and

a controller including a CMOS transistor disposed on the P-type semiconductor substrate and including a P-channel MOS transistor formed in an N-type region formed in the P-type  
10 semiconductor substrate on the main surface of the P-type semiconductor substrate and an N-channel MOS transistor formed in a P-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from  
15 the P-type semiconductor substrate by the N-type region,

wherein the controller is configured to compare an output voltage from the output transistor with a reference voltage and provide feedback such that the output voltage remains constant.

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16. The semiconductor device as defined in Claim 15, wherein the P-type semiconductor substrate comprises a P-type high concentration semiconductor substrate and a first P-type low concentration epitaxial layer, the P-type high  
25 concentration semiconductor substrate being disposed opposite to the main surface of the P-type semiconductor substrate,

and the first P-type low concentration epitaxial layer being disposed over the P-type high concentration semiconductor substrate.

5           17.    The semiconductor device as defined in Claim 16, wherein the N-type region comprises a bottom portion including an N-type buried layer which is disposed at an interface of the P-type high concentration semiconductor substrate and the first P-type low concentration epitaxial  
10   layer.

          18.    The semiconductor device as defined in Claim 17, wherein the N-type region further comprises at least two side portions, each including an Nwell region, to form a structure  
15   such that the P-type region is surrounded by the Nwell regions and the N-type buried layer.

          19.    The semiconductor device as defined in Claim 16, wherein the first P-type low concentration epitaxial layer  
20   includes a P-type buried layer disposed under a region where the source of the P-channel DMOS transistor is formed.

          20.    A semiconductor device, comprising:  
          a fixed voltage circuit, comprising:  
25   a P-type semiconductor substrate including a P-type high concentration semiconductor substrate, a first P-type low

concentration epitaxial layer, and a second P-type low concentration epitaxial layer, the P-type high concentration semiconductor substrate being disposed opposite to a main surface of the P-type semiconductor substrate, the second P-type low concentration epitaxial layer being disposed over the P-type high concentration semiconductor substrate, and the first P-type low concentration epitaxial layer being disposed over the second P-type low concentration epitaxial layer;

an output transistor including a P-channel DMOS transistor disposed on the P-type semiconductor substrate and including a drain formed of the P-type semiconductor substrate and a source formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, and

a controller including a CMOS transistor disposed on the P-type semiconductor substrate and including a P-channel MOS transistor formed in an N-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate and an N-channel MOS transistor formed in a P-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from the P-type semiconductor substrate by the N-type region,

wherein the N-type region comprises a bottom portion including an N-type buried layer which is disposed at an interface of the first P-type low concentration epitaxial

layer and the second P-type low concentration epitaxial layer.

21. A semiconductor device, comprising:

a fixed voltage circuit, comprising:

5 a P-type semiconductor substrate including a P-type semiconductor substrate including a P-type high concentration semiconductor substrate, a first P-type low concentration epitaxial layer, a second P-type low concentration epitaxial layer, and a third P-type low concentration epitaxial layer, the P-type high concentration semiconductor substrate being  
10 disposed opposite to a main surface of the P-type semiconductor substrate, the second P-type low concentration epitaxial layer being disposed over the P-type high concentration semiconductor substrate, the third P-type low concentration epitaxial layer being disposed over the second  
15 P-type low concentration epitaxial layer, and the first P-type low concentration epitaxial layer being disposed over the third P-type low concentration epitaxial layer;

an output transistor including a P-channel DMOS transistor  
20 disposed on the P-type semiconductor substrate and including a drain formed of the P-type semiconductor substrate and a source formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate; and

a controller including a CMOS transistor disposed on the  
25 P-type semiconductor substrate and including a P-channel MOS transistor formed in an N-type region formed in the P-type

semiconductor substrate on the main surface of the P-type semiconductor substrate and an N-channel MOS transistor formed in a P-type region formed in the P-type semiconductor substrate on the main surface of the P-type semiconductor substrate, the P-type region being electrically isolated from the P-type semiconductor substrate by the N-type region, wherein the N-type region comprises a bottom portion including an N-type buried layer which is disposed at an interface of the second P-type low concentration epitaxial layer and the third P-type low concentration epitaxial layer, and the P-type buried layer is disposed on a bottom of the P-type region disposed at an interface of the first P-type low concentration epitaxial layer and the third P-type low concentration epitaxial layer.

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22. A method of forming a semiconductor device, comprising the steps of:

forming a first P-type low concentration epitaxial layer over a P-type high concentration semiconductor substrate;

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implanting an N-type impurity into a CMOS formation region of the first P-type low concentration epitaxial layer to form an N-well region;

implanting a P-type impurity into an NchMOS transistor formation region of the first P-type low concentration epitaxial layer to form a Pwell region;

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forming LOCOS oxide layers on the first P-type low concentration epitaxial layer;

forming a first gate oxide layer on the Nwell region;

forming a second gate oxide layer on the Pwell region;

5 forming a third gate oxide layer on the first P-type low concentration epitaxial layer;

performing channel doping implant into the Nwell region and the Pwell region;

depositing a polysilicon layer over the semiconductor  
10 substrate, which in turn has disposed thereon an oxide layer to form an N-type polysilicon layer;

patterning the polysilicon layer to form a first gate electrode, a second gate electrode in the NchMOS transistor formation region, and a third gate electrode;

15 masking the third gate electrode to selectively implant an N-type impurity into the first P-type low concentration epitaxial layer of the PchDMOS transistor formation region;

performing thermal processing to form a first N-channel diffusion layer;

20 masking the first and third gate electrodes to selectively implant a P-type impurity into source formation regions in the first Nwell region of the PchMOS transistor formation region, the first N-channel diffusion layer of the PchDMOS transistor formation region, and the first and third  
25 gate electrodes;

masking the second gate to selectively implant an N-

type impurity into the first Pwell region of the NchMOS transistor formation region and the N-type high concentration diffusion layer formation region of the first N-channel diffusion layer in the PchDMOS transistor formation region;

5 performing thermal processing to form the first P-type high concentration diffusion layers, N-type high concentration diffusion layers on the Pwell region, and the first N-type high concentration diffusion layer and the second P-type high concentration diffusion layers on the  
10 first N-channel diffusion layer.

23. A semiconductor device, comprising:

a first-polarity-type semiconductor substrate;

a first-polarity-channel DMOS transistor disposed on  
15 the first-polarity-type semiconductor substrate and including a drain formed of the first-polarity-type semiconductor substrate and a source formed in the first-polarity-type semiconductor substrate on a main surface of the first-polarity-type semiconductor substrate; and

20 a CMOS transistor disposed on the first-polarity-type semiconductor substrate and including a first-polarity-channel MOS transistor formed in a second-polarity-type region formed in the first-polarity-type semiconductor substrate on the main surface of the first-polarity-type  
25 semiconductor substrate and a second-polarity-channel MOS transistor formed in a first-polarity-type region formed in



the first-polarity-type semiconductor substrate on the main surface of the first-polarity-type semiconductor substrate, the first-polarity-type region being electrically isolated from the first-polarity-type semiconductor substrate by the  
5 second-polarity-type region.